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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/438,247	11/12/1999	JUNJI NISHIGAKI	15162/01290	9067

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EXAMINER	
KASSA, YOSEF	

ART UNIT	PAPER NUMBER
2625	8

DATE MAILED: 08/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/438,247	NISHIGAKI ET AL.	
	Examiner	Art Unit	
	YOSEF KASSA	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Response to Arguments

1. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hino et al (5,117,468), and further in view of Horiguchi (4,680,643).

With regard to claim 1, Hino et al discloses a plurality of processors processing input image data (see col. 2, lines 21-25, a plurality of local image extracting circuits of extracting a plurality of pixel data), in parallel with each other and outputting respective processed image data (see col. 2, lines 35-39, the local image reconstruction means in parallel, to deliver a plurality of modified pixel data).

Hino et al did not explicitly call for an address memory storing address information for each respective image data processed by each of plurality of processors. However, Horiguchi (see col. 3, lines 40-49) teaches this feature. Hino et al and Horiguchi are combinable because they from the same field of endeavor, that is, image combining process (see abstract or Horiguchi). At the time of the invention, it would have been obvious to incorporate the teaching of Horiguchi's segment image

processing system into Hino et al system. The motivation for doing so is to provide an image display apparatus in which one picture plane is divided and a plurality of desired image can be easily displayed (see col. 1, lines 65-68 of Horiguchi's).

With regard to claim 2, Hino et al discloses an image memory storing image data output from plurality of processors (see col. 2, 42-46), and read means reading image data from image memory on the basis of address information stored in address memory (col. 2, lines 45-47).

With regard to claim 3, Hino et al discloses an image memory storing image data output from plurality of processors along the sequence of addresses on the basis of address information stored in address memory (see col. 2, lines 42-47).

With regard to claim 4, Hino et al discloses input means inputting image data subjected to processing in synchronization with a first external device, and output means outputting image data processed in plurality of processors and address information stored in address memory in synchronization with a second external device (see col. 5, lines 5-16).

With regard to claim 5, Hino et al discloses plurality of processors also output arrangement information corresponding to processed data when outputting data (see col. 2, lines 38-44).

With regard to claim 6, Hino et al discloses a plurality of processors performing prescribed processing on a plurality of data divided from single image data respectively (see col. 2, lines 21-25, extracting a plurality of pixel data having a predetermined positional relation on a two-dimensional original image); and a controller restoring a

single image from plurality of data processed in plurality of processors in accordance with arrangement information (see col. 2, lines 52-59, the local image reconstruction means, the local image processing circuits and first and second image data transfer means are incorporated in, for example, a single image processor, and a control processor).

Hino et al did not explicitly call for a first memory storing arrangement information in original image data for plurality of divided data. However, Horiguchi (see col. 3, lines 6-14) teaches this feature. Hino et al and Horiguchi are combinable because they from the same field of endeavor, that is, segmented image combining (see abstract of Horiguchi). At the time of the invention, it would have been obvious to incorporate the teaching of Horiguchi's segmented image storing system into Hino et al system. The motivation for doing so is to store segment addresses indicative of a plurality of selected image data of one picture plane (see col. 2, lines 15-20 of Horiguchi's).

With regard to claim 7, Hino et al discloses including a second memory storing data processed in plurality of processors, wherein controller reacts data from second memory in sequence along arrangement information and restores image (see col. 2, lines 38-46).

With regard to claim 8, Hino et al discloses including an image memory, wherein controller stores processed data in positions of image memory corresponding to arrangement information (see col. 2, lines 21-26).

With regard to claim 9, Hino et al discloses first memory is provided in correspondence to each of plurality of processors (see col. 2, lines 38-40).

With regard to claim 10, Hino et al discloses plurality of processors also output arrangement information corresponding to processed data when outputting data (see col. 2, lines 40-46).

Claim 11 is similarly analyzed as claim 6. As to the additional limitation of restoring an image on accordance with address information that indicates an arrangement of the divided data (see col. 2, lines 31-43 of Horiguchi).

Other Prior Art Cited

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent No. (5,142,616) Kellas et al discloses electronic graphic system.

US Patent No. (5,646,679) Yano et al discloses image combining method and apparatus.

US Patent No. (5,920,674) Pkita et al discloses video signal editing apparatus.

US Patent No. (5,692,210) Mita et al discloses image processing apparatus having parallel processors...

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOSEF KASSA whose telephone number is (703) 306-

5918. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, BHAVESH MEHTA can be reached on (703) 308-5246. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 872-9314 for regular communication and (703) 872-9314 for after Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the customer service office whose telephone number is (703) 306-5631. The group receptionist number for TC 2600 is (703) 305-4700.

PATENT EXAMINER

Yosef Kassa

08/06/03.

BHAVESH M. MEHTA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600